Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **CD+**
2. **TIME CHANNEL INPUT +**
3. **SET HYSTERESIS**
4. **V REF**
5. **N/C**
6. **AMP IN +**
7. **AMP IN –**
8. **N/C**
9. **VCC**
10. **SET PULSE WITH**
11. **READ/WRITE**
12. **TIME PULSE OUT**
13. **TIME PULSE IN**
14. **ENCODED DATA OUTPUT**
15. **CHANNEL ALIGNMENT OUTPUT**
16. **CAGC**
17. **DIGITAL GND**
18. **AMP OUT +**
19. **AMP OUT –**
20. **ANALOG GND**
21. **GATE CHANNEL INPUT**
22. **GATE CHANNEL INPUT**
23. **TIME CHANNEL INPUT –**
24. **CD -**

**3 2 1 24 23 22**

**10 11 N/C 12 13 14 15**

**21**

**20**

**19**

**18**

**N/C**

**17**

**16**

**4**

**N/C**

**N/C**

**6**

**7**

**N/C**

**9**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .091” X .098” DATE: 9/23/21**

**MFG: NATIONAL THICKNESS .025” P/N: DP8464B-2**

**DG 10.1.2**

#### Rev B, 7/19/02